

GSG 勁力 半導體

Gunter Semiconductor GmbH

TFB3869

EDITION 09/00

One Chip Subscriber Line Interface (SLIC)

For inquiry please contact :

China

Tel: 0086-755-3200442

Fax: 0086-755-3355520

Hong Kong

Tel : 00852-26190748

Fax: 00852-24948080

e-mail

sales@gsg-asia.com

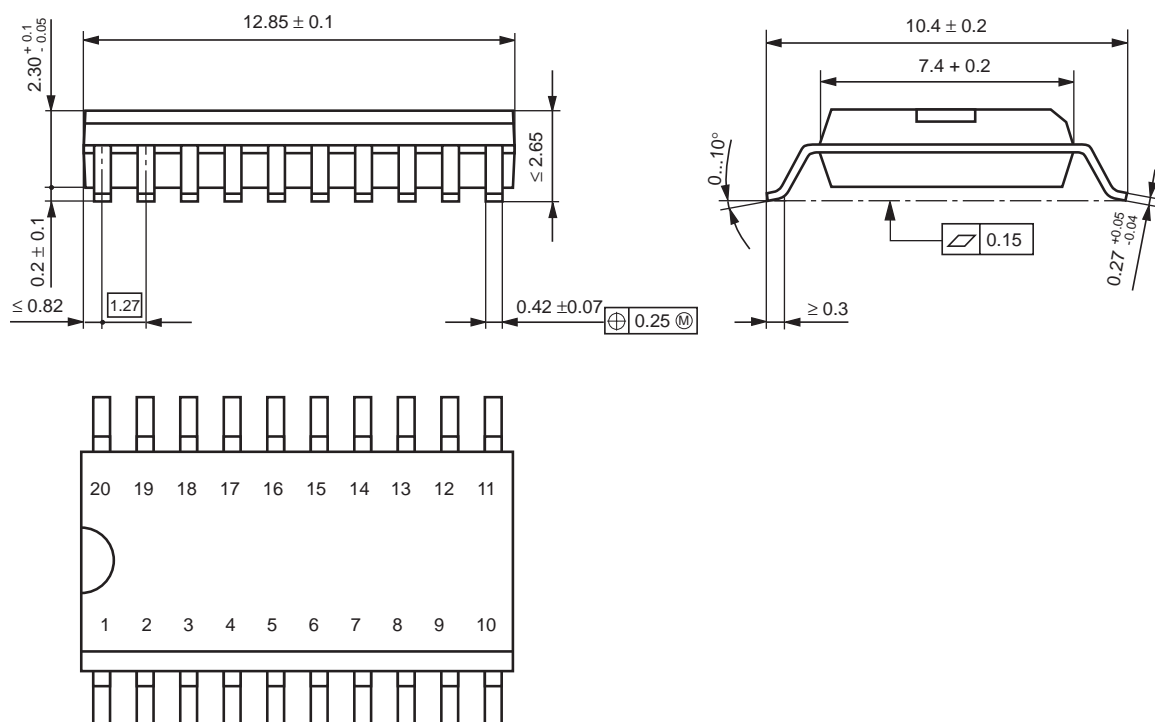
Subscriber Line Interface Circuit (SLIC)

Features

- High balance without external precession devices
- Low supply current
- Direct coupling with standard CODECs
- Subscriber feeding by integrated constant current sources
- Programmable constant current by external resistor
- Hybrid function, programmable via external components
- Logic output for ground key detection
- Logic output for loop current detection

Package

- SOP 20



Pin Configuration

1	-HK	Negative output for transmitter direction
2	n. c.	This pin is internally used. It is not permitted to connect any external components.
3	ISET	Control input for loop current
4	ZOUT	Output, network for hybrid function
5	ZIN	Input, network for hybrid funktion
6	ET	Output, ground key detection
7	LD	Output, loop current detection
8	LA	Line output
9	n. c.	This pin is internally used. It is not permitted to connect any external components.
10	VBAT	Negative supply voltage
11	LB	Line output
12	n. c.	This pin is internally used. It is not permitted to connect any external components.
13	GND	Ground
14	n.c.	This pin is internally used. It is not permitted to connect any external components.
15	+CR	External capacitor for AC/DC selction
16	-CR	External capacitor for AC/DC selction
17	+MIC	Positive input for receive direction
18	-MIC	Negative input for receive direction
19	VCC	Positive supply voltage
20	+HK	Positive output for transmitter direction

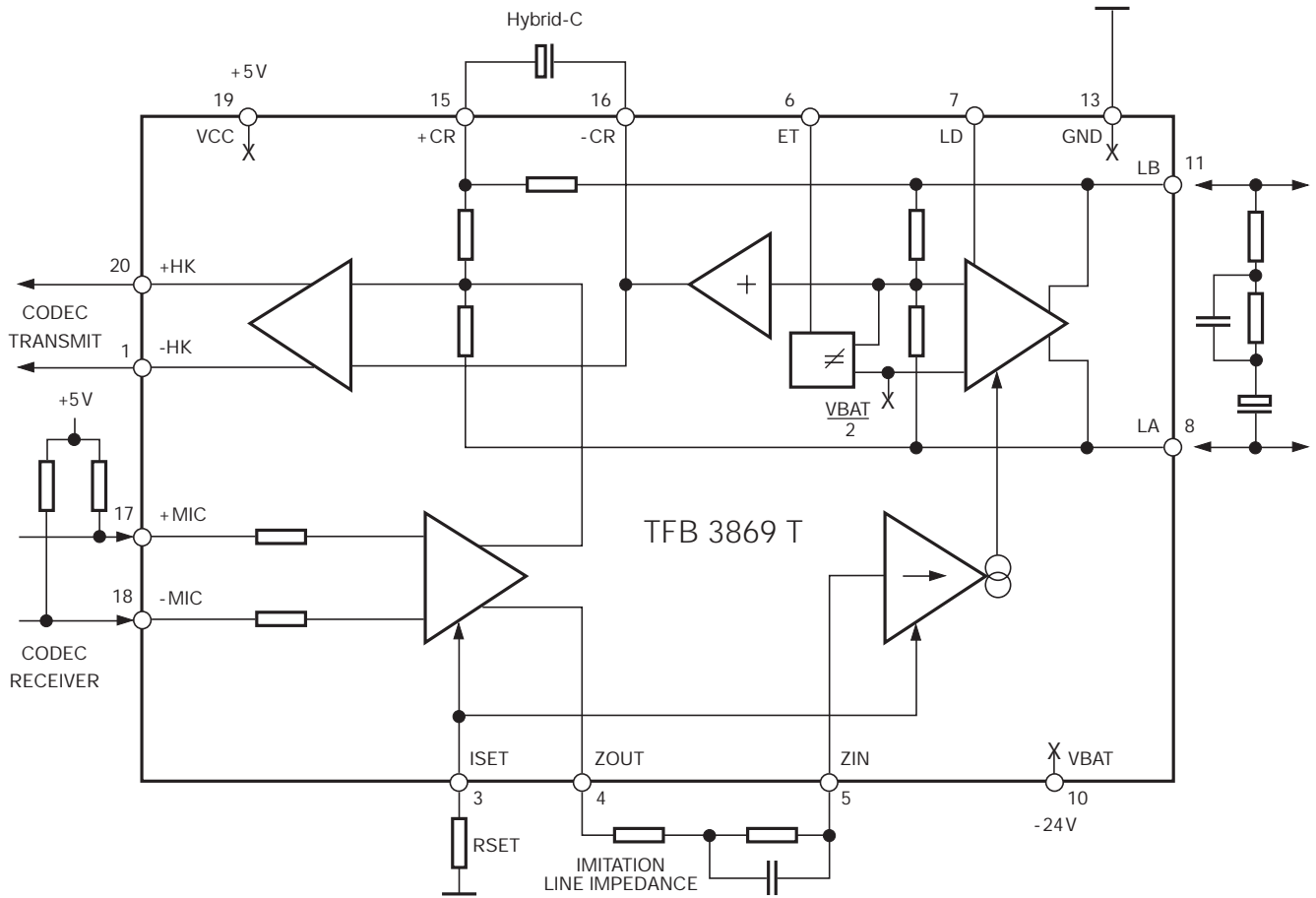
Pin Description

VBAT	Supply voltage -24 V
VCC	Supply voltage +5 V
GND	Ground
ISET	Control input for loop current Voltage drop on grounded resistor of 23,3 V.
LA, LB	Subscriber line, $I_{LA/LB} = 120 (I_{SET}) = 120 \cdot \frac{23.3 \text{ V}}{R_{SET}}$ The subscriber line current is determined by the ISET current.
+MIC; -MIC	Differential input for the receive direction The input resistance is 10 k Ω per pin, the output voltage in receive direction line is four times the MIC voltage.
+HK; -HK	Differential output for the transmitter direction with unit gain of the input signal of the subscriber line with common mode offset voltage of + 2.5 V
ZIN	Current node input for hybrid amplifier $Z_{NB} = 50$ (sum)
ZOUT	Driver output for hybrid function
ET	Logic output for ground key detection (low-aktiv)
LD	Logic output for loop current detection (low-aktiv)
+CR; -CR	External capacitor for hybrid function

All Pin are ESD protected except PIN 2, 9, 12 and 14.

Pin	Symbol	Circuit	Pin	Symbol	Circuit
1	-HK		7	LD	
3	ISET		8	LA	
4	ZOUT		11	LB	
5	ZIN		17 18	+MIC -MIC	
6	ET		20	+HK	

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings $T_a = 0^\circ\text{C}$ up to 70°C	Symbol	Min.	Max.	Unit
Positive supply voltage	+5V	0	5.25	V
Negative supply voltage	-24V	-25.25	0	V
All other pins		Pin10 - 0.3	Pin19 + 0.3	V
Junction temperature	T_j	-	150	$^\circ\text{C}$

Electrical Characteristics

DC Characteristics

$V_{BAT} = -24\text{ V}$, $V_{CC} = +5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$

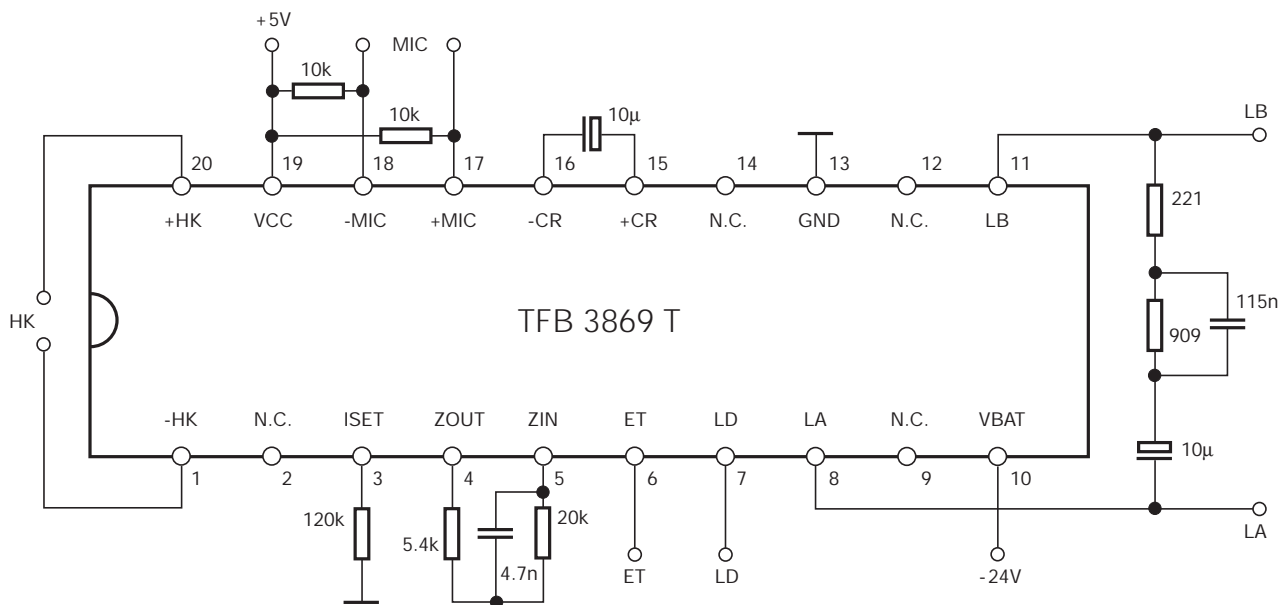
Parameter	Symbol	Min.	Max.	Unit
Supply current	I_{CC}	-	1.0	mA
Loop current	I_{SCHL}	20	24	mA
Supply current	$I_{BAT}-I_{SCHL}$	-3	-	mA
Symmetrical voltage	V_{SYM}	11	13	V
Biaspoint +HK	V_{+HK}	2	3	V
Biaspoint -HK	V_{-HK}	2	3	V
Offset HK	$V_{+HK} - V_{-HK}$	-250	250	mV
LD-detection (low) $I_{LD} = 200\text{ }\mu\text{A}$	V_{LD}	-	0.4	V
LD-detection (high) $V_{LD} = 5\text{ V}$	I_{LD}	-	2	μA
ET-detection (low) $I_{ET} = 200\text{ }\mu\text{A}$	V_{ET}	-	0.4	V
ET-detection (high) $V_{ET} = 5\text{ V}$	I_{ET}	-	2	μA

AC Characteristics

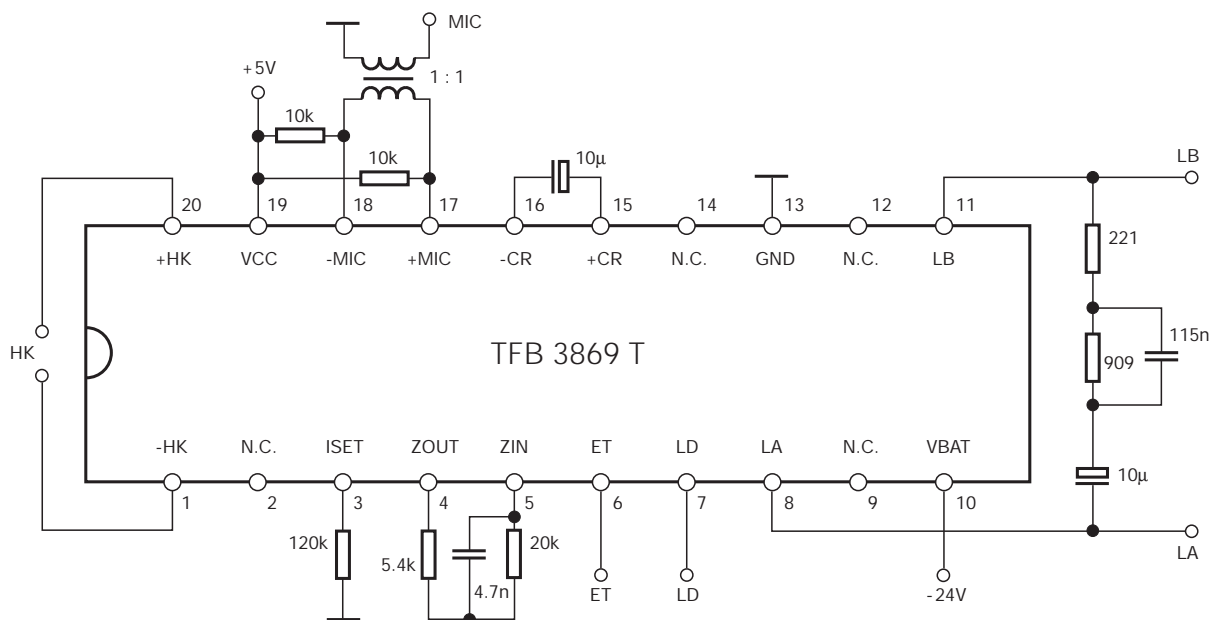
$V_{BAT} = -24\text{ V}$, $V_{CC} = +5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Min.	Max.	Unit
Balance two wire	a_{2-2}	54	-	dB
Balance two wire to four wire	a_{2-4}	58	-	dB
Loss MIC/HK	$a_{MIC/HK}$	12	-	dB
Gain for receiver direction	G_R	10.5	13.5	dB
Gain for transmitter direction	G_T	-7.5	-4.5	dB

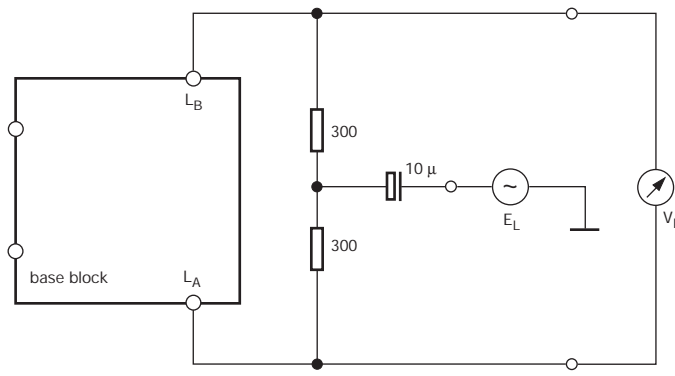
Application Circuit



Test Circuit, Base Block

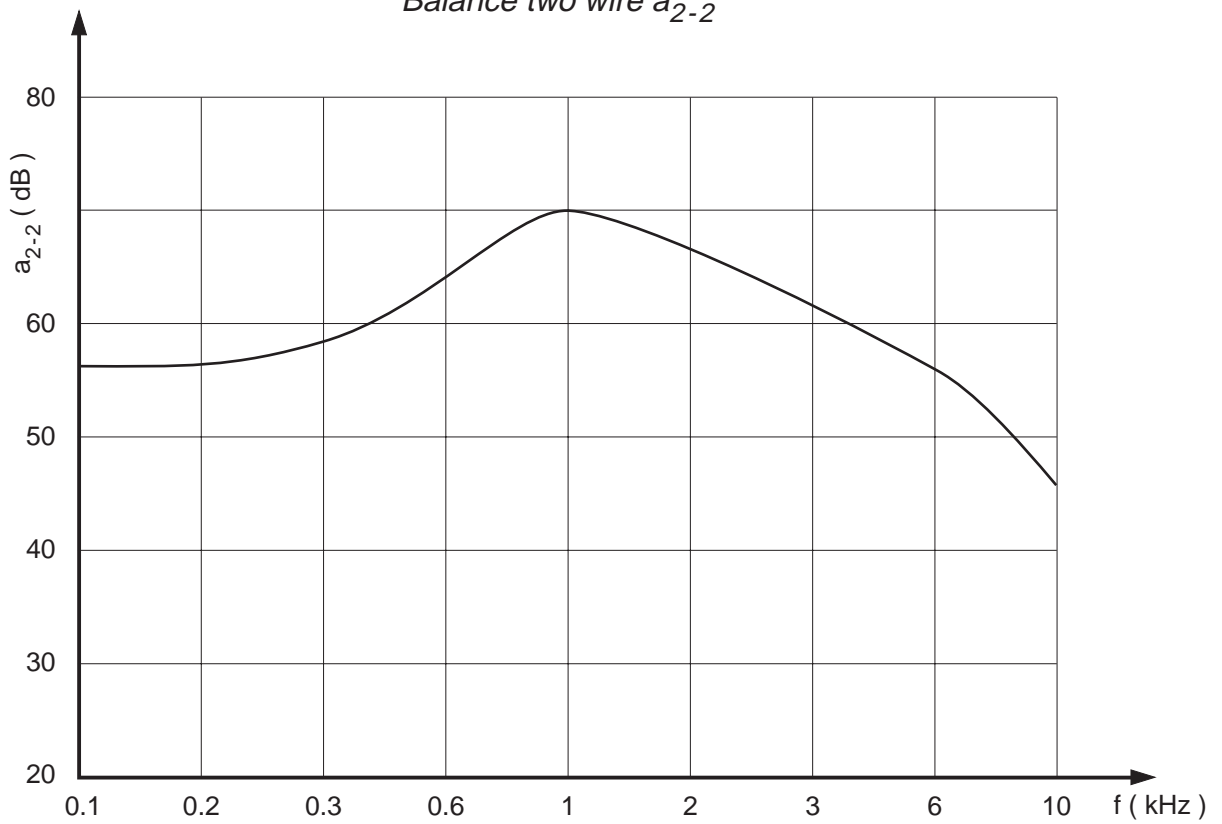


Test Circuit, Balance, Two Wire

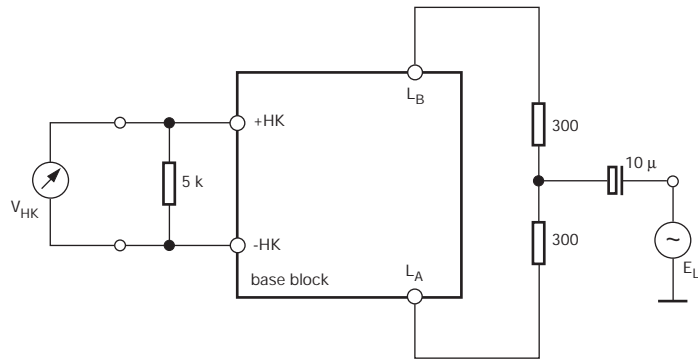


$$a_{2-2} = 20 \log \left| \frac{E_L}{V_L} \right|$$

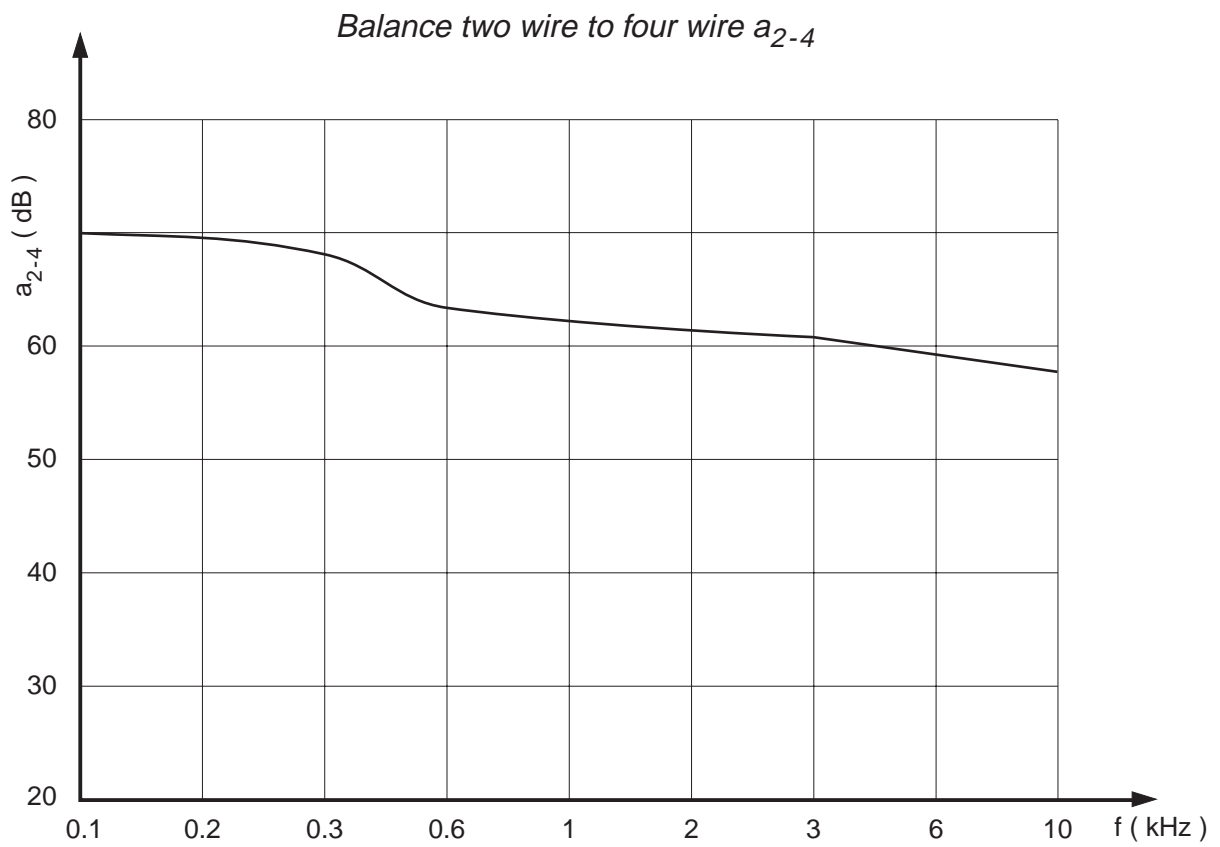
Balance two wire a_{2-2}



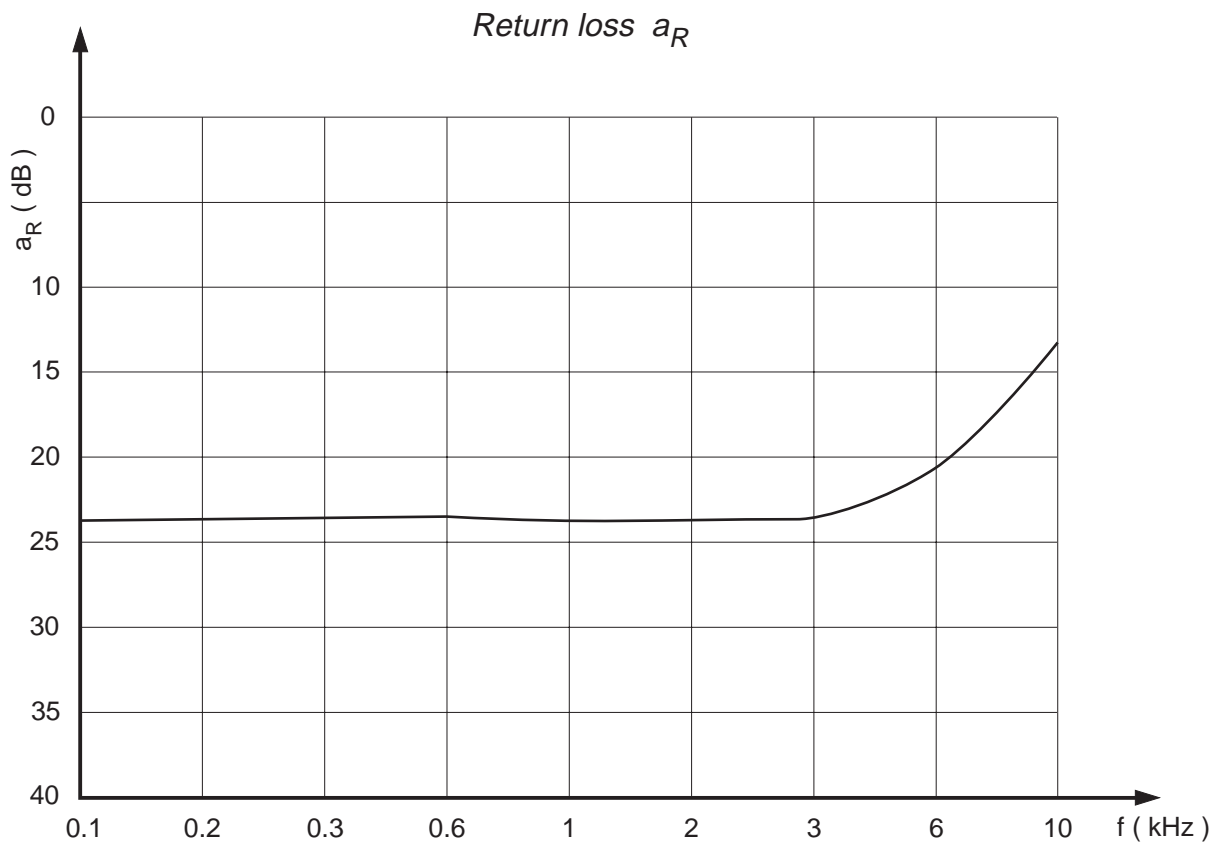
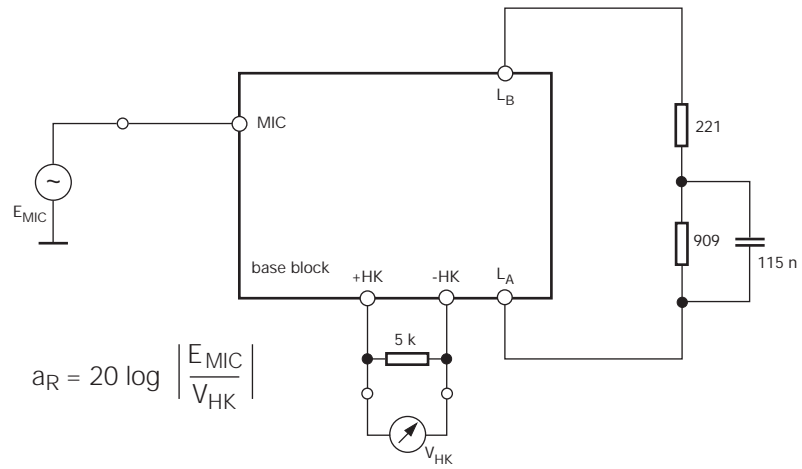
Test Circuit, Balance Two Wire To Four Wire



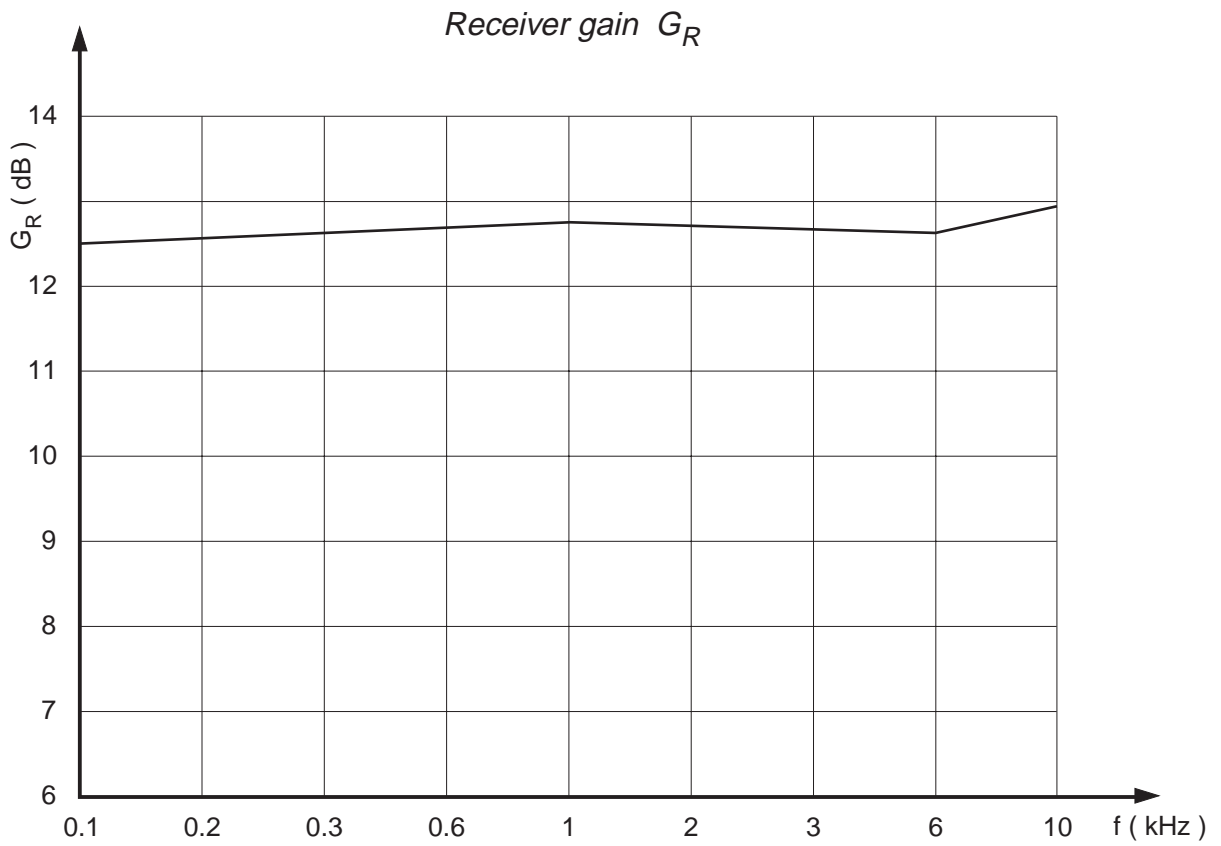
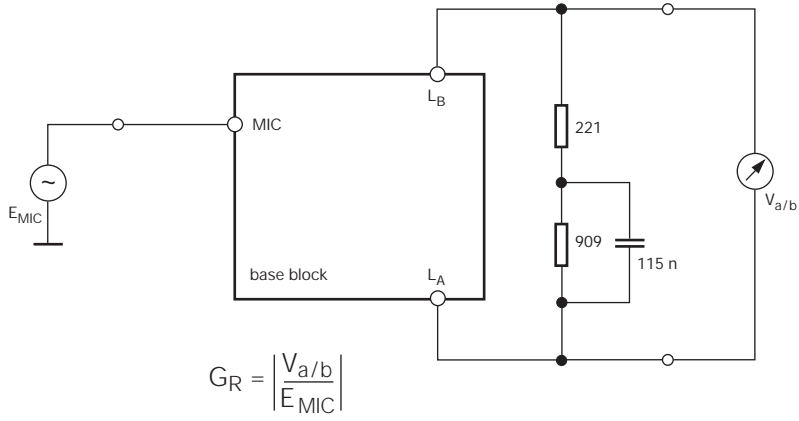
$$a_{2-4} = 20 \log \left| \frac{E_L}{V_{HK}} \right|$$



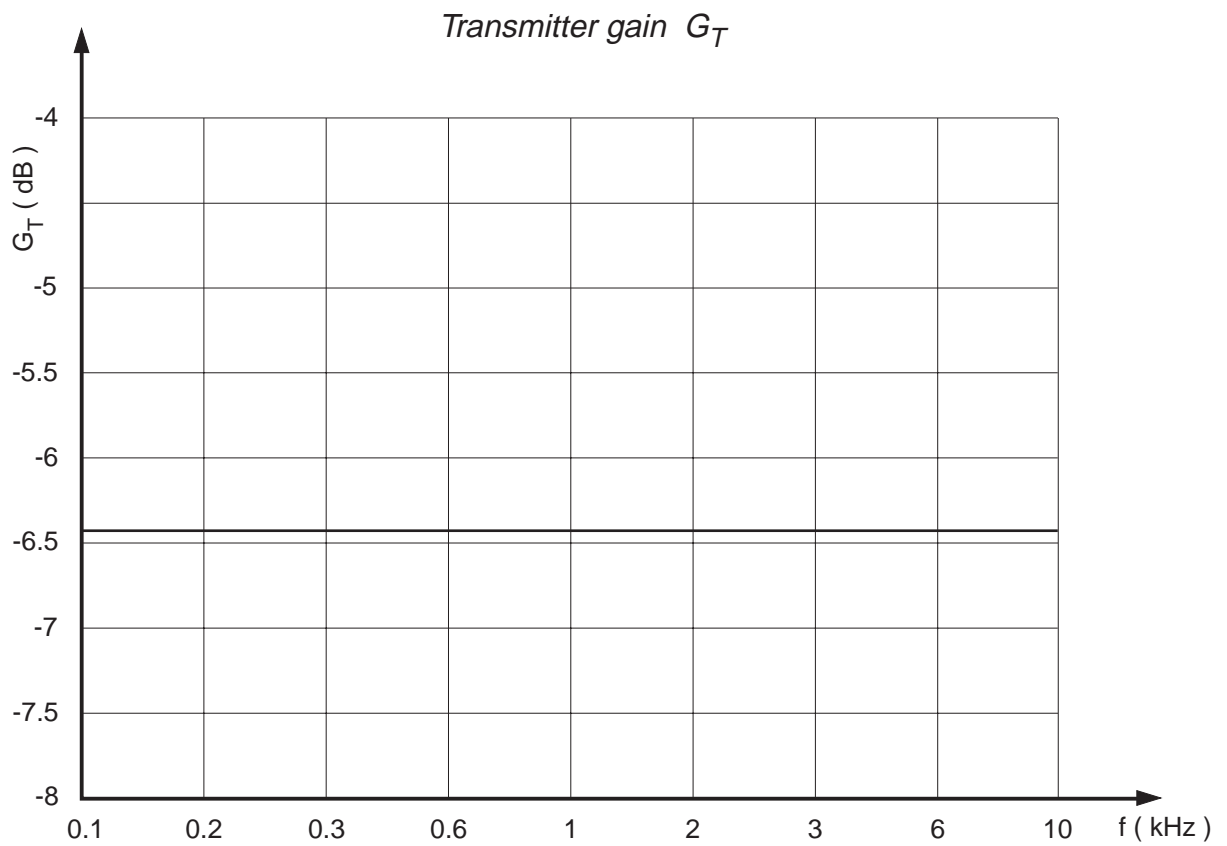
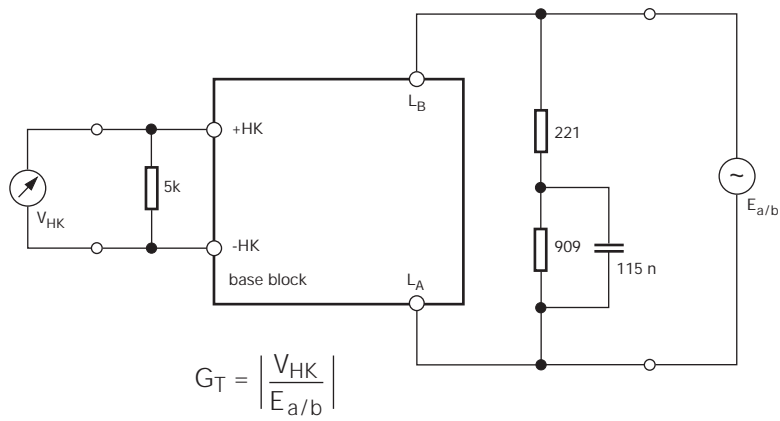
Test Circuit, Return Loss



Test Circuit, Receiver Gain



Test Circuit, Transmitter Gain



Loop Conditions

Loop conditions	LD	ET
Loop connected, no ground key	High	High
Loop connected, ground key aktiv	High	Low
Loop disconnected, no ground key	Low	High

Loop Detection

Condition for switching of the logic output LD:

$$I_{SCHL} * R_L = V_{BAT} - 5V$$

Status of the logic output LD depending on loop current:

$$LD = \text{Low}$$

$$I_{SCHL} * R_L > V_{BAT} - 5V$$

$$LD = \text{High}$$

$$I_{SCHL} * R_L < V_{BAT} - 5V$$

Loop Resistance

The useable loop resistance can be calculated as follows:

$$R_L < \frac{(V_{BAT} - 5V)}{I_{SCHL}}$$

$$R_L < \frac{(V_{BAT} - 5V)}{120 * 23.3V} * R_{SET}$$

In accordance with the conditions mentioned above a reliable loop detection will be guaranteed for a closed loop resistance value lower than 815 Ω .

Ground Key Detection

For ground key detection the LA or LB outputs have to be connected to ground. In this case the voltage drop on an internal differential amplifier reaches 1 V in minimum for switching the ET output from high to low.

Protection Circuit

